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CLAIMS

We claim:

1. A packaged semiconductor device comprising:

a plurality of external connectors;

a system chip connected to at least a first group of said plurality of external connectors; and

a memory chip connected to said system chip through a data bus, said memory chip comprising:

a plurality of data buffers for transferring data between said memory chip and said data bus; and

at least one test buffer connected to at least a first group of said plurality of data buffers; wherein said at least one test buffer is connected to certain of said first group of said plurality of external connectors to provide testing of said memory chip while contained within said packaged semiconductor device.

2. The packaged semiconductor device of Claim 1, wherein said memory chip comprises at least one of a random access memory (RAM), a static RAM, a dynamic RAM, a non-volatile RAM, a read only memory (ROM), a programmable ROM, an erasable programmable ROM, an electrically erasable programmable ROM, and a flash memory.

3. The packaged semiconductor device of Claim 1, wherein said system chip comprises at least one of a processor, a microcontroller, a microprocessor, a field programmable gate array, and an application specific integrated circuit.

4. The packaged semiconductor device of Claim 1, wherein said memory chip comprises at least an eight bit dynamic random access memory which communicates with said system chip through said data bus having a bus width equal to or greater than the number of bits of said memory chip.

5. The packaged semiconductor device of Claim 4, wherein said memory chip comprises a 128 bit dynamic random access memory which communicates with said system chip through said data bus having a bus width of at least 128 bits.

6. The packaged semiconductor device of Claim 1, wherein said at least one test buffer further comprises providing data compression such that the required number of said test buffers is less than the number of said data buffers.

7. The packaged semiconductor device of Claim 1, wherein a ratio of said data buffers to said test buffers is greater than or equal to 2:1.

8. The packaged semiconductor device of Claim 1, wherein said at least one test buffer is disabled during normal operation of said memory chip, said at least one test buffer enabled upon receipt of a memory test signal, wherein said at least one test buffer provides said memory chip with at least one of addresses, control signals, and data input.

9. The packaged semiconductor device of Claim 1, wherein said at least one test buffer communicates with external memory test equipment through said certain of said first group of said plurality of external connectors to test said memory chip contained within said packaged semiconductor device.

10. The packaged semiconductor device of Claim 1, wherein said memory chip and said system chip are formed as a single chip.

11. The packaged semiconductor device of Claim 1, wherein at least one of said plurality of data buffers incorporates said at least one test buffer.

12. A method of testing a memory within a packaged semiconductor device, said method comprising:

providing a plurality of connectors on said packaged semiconductor device to connect to external components;

providing system circuitry connected to at least a first group of said plurality of connectors;

providing memory circuitry connected to said system circuitry through a data bus, said memory circuitry further providing:

data buffers for transferring data between said memory circuitry and said data bus; and

at least one test buffer connected to at least a first group of said data buffers and connected to certain of said first group of said plurality of external connectors to provide testing of said memory circuitry while contained within said packaged semiconductor device.

13. The method of Claim 12, further comprising providing said memory circuitry and said system circuitry on a single chip within said packaged semiconductor device.

14. The method of Claim 12, further comprising providing said memory circuitry and said system circuitry on separate chips within said packaged semiconductor device.

15. The method of Claim 12, further comprising providing said data bus with a bus width equal to or greater than the number of bits of said memory circuitry.

16. The method of Claim 12, further comprising providing data compression for said at least one test buffer such that the number of said test buffers required is less than the number of said data buffers.

17. The method of Claim 12, further comprising disabling said at least one test buffer during normal operation of said memory circuitry, said at least one test buffer enabled upon receipt of a memory test signal, wherein said at least one test buffer providing said memory circuitry with at least one of addresses, control signals, and data input.

18. The method of Claim 12, further comprising utilizing said at least one test buffer to communicate with external memory test equipment through said certain of said first group of said plurality of external connectors to test said memory circuitry contained within said packaged semiconductor device.

19. A semiconductor memory chip comprising:

a memory storage array for storing data;

a plurality of data buffers for writing data to or reading data from said memory storage array; and

at least one test buffer connected to at least a first group of said plurality of data buffers, said at least one test buffer providing testing of said memory chip.

20. The chip of Claim 19, wherein said memory chip comprises at least one of a random access memory (RAM), a static RAM, a dynamic RAM, a non-volatile RAM, a read only memory (ROM), a programmable ROM, an erasable programmable ROM, an electrically erasable programmable ROM, and a flash memory.

21. The chip of Claim 19, wherein said at least one test buffer further comprises providing data compression such that the required number of said test buffers is less than the number of said data buffers.

22. The chip of Claim 19, wherein said at least one test buffer is disabled during normal operation of said memory chip, said at least one test buffer enabled upon receipt of a memory test signal, wherein said at least one test buffer provides said memory chip with at least one of addresses, control signals, and data input.

23. The chip of Claim 19, wherein said at least one test buffer communicates with external memory test equipment through connectors to test said memory chip contained within a packaged semiconductor device.

24. The chip of Claim 19, wherein at least one of said plurality of data buffers incorporates said at least one test buffer.

25. A packaged semiconductor device comprising:

a plurality of external connectors;

a primary chip connected to at least a first group of said plurality of external connectors; and

a secondary chip connected to said primary chip, said secondary chip comprising:

a plurality of signal drivers for transferring information between said secondary chip and said primary chip; and

at least one test signal driver connected to at least a first group of said plurality of signal drivers, wherein said at least one test signal driver is connected to certain of said first group of said plurality of external connectors to provide testing of said secondary chip while contained within said packaged semiconductor device.

26. The packaged semiconductor device of Claim 25, wherein said secondary chip comprises at least one of a memory chip, a co-processor chip, an analog subsystem, and an application-specific subsystem.

27. The packaged semiconductor device of Claim 25, wherein said primary chip comprises at least one of a processor, a microcontroller, a microprocessor, a field programmable gate array, and an application specific integrated circuit.

28. The packaged semiconductor device of Claim 25, wherein said at least one test signal driver is operable to comprise data such that the required number of said test signal drivers is less than the number of said data signal drivers.

29. The packaged semiconductor device of Claim 25:

wherein said at least one test signal driver is disabled during normal operation of said secondary chip and enabled during a test mode;

wherein said at least one test signal driver provides said secondary chip with at least one of addresses, control signals, and data input.

30. The packaged semiconductor device of Claim 25, wherein said at least one test signal driver communicates with external test equipment through said certain of said first group of said plurality of external connectors to test said secondary chip contained within said packaged semiconductor device.

31. The packaged semiconductor device of Claim 25, wherein said secondary chip and said primary chip are formed as a single chip.

32. A method of testing a chip within a packaged semiconductor device, said method comprising:

providing a plurality of connectors on said packaged semiconductor device to connect to external components;

providing primary circuitry connected to at least a first group of said plurality of connectors;

providing secondary circuitry connected to said primary circuitry, said secondary circuitry further providing:

signal drivers for transferring information between said secondary circuitry and said primary circuitry; and

at least one test signal driver connected to at least a first group of said signal drivers and connected to certain of said first group of said plurality of external connectors to provide testing of said secondary circuitry while contained within said packaged semiconductor device.

33. The method of Claim 32, further comprising providing said secondary circuitry and said primary circuitry on a single chip within said packaged semiconductor device.

34. The method of Claim 32, further comprising providing said secondary circuitry and said primary circuitry on separate chips within said packaged semiconductor device.

35. The method of Claim 32, further comprising providing data compression for said at least one test signal driver such that the number of said test signal drivers required is less than the number of said signal drivers.

36. The method of Claim 32, further comprising disabling said at least one test signal driver during normal operation of said secondary circuitry, and enabling said at least one test signal driver during test mode, wherein said at least one test signal driver provides said secondary circuitry with at least one of addresses, control signals, and data input.

37. The method of Claim 32, further comprising utilizing said at least one test signal driver to communicate with external test equipment through said certain of said first group of said plurality of external connectors to test said secondary circuitry contained within said packaged semiconductor device.

38. A semiconductor chip for incorporation as a secondary chip into a multi-chip packaged semiconductor device, the semiconductor chip comprising:

a data buffer operable to connect to a primary chip incorporated into the multi-chip packaged semiconductor device for receiving from and outputting signals to the primary chip; and

a test buffer operable to directly connect to an external terminal of the multi-chip packaged semiconductor device for receiving from and outputting signals to external testing circuitry.

39. The semiconductor chip of Claim 38, wherein during a test mode for the semiconductor chip, at least a portion of the data buffer is tri-stated and the test buffer is enabled to provide testing for the semiconductor chip.

40. The semiconductor chip of Claim 38, wherein during a normal operation for the semiconductor chip, the data buffer is enabled and the test buffer is tri-stated.